Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 70059

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JAN. / FEB. 2026
First Semester
VLSI Design
P23VDE03 – FOUNDATIONS OF VLSI CAD
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Define combinatorial optimization in the context of VLSI CAD.	2	K1	CO1
2.	Outline the significance of tractable problems in VLSI design automation.	2	K2	CO1
3.	Infer how constraint graphs can be applied to perform layout compaction.	2	K2	CO2
4.	List any two partitioning strategies used in placement.	2	K1	CO2
5.	Compare and contrast channel routing and area routing.	2	K2	CO3
6.	Interpret the role of shape functions in floor plan sizing with a simple example.	2	K2	CO3
7.	Illustrate the difference between gate-level simulation and switch-level simulation.	2	K2	CO4
8.	Explain Binary Decision Diagrams (BDDs) and describe one practical application where they are used.	2	K2	CO4
9.	Identify the purpose of allocation in high-level synthesis.	2	K2	CO5
10.	Summarize the role of high-level transformations in synthesis.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Analyze the influence of algorithmic graph theory on partitioning and placement decisions in VLSI CAD.	13	K4	CO1

(OR)

	b)	Inspect various steps of solving an intractable optimization problem in VLSI automation and compare with a tractable alternative.	13	K4	CO1
12.	a)	Dissect the operation of a constraint-graph compaction algorithm and highlight how it reduces layout area.	13	K4	CO2
		(OR)			
	b)	Analyze the strengths and limitations of partitioning algorithms in handling complex circuits with high interconnect density.	13	K4	CO2
13.	a)	Evaluate the efficiency of shape-function based floor planning by considering trade-offs in area and wire length.	13	K5	CO3
		(OR)			
	b)	Judge the effectiveness of global routing algorithms in preventing routing congestion for large-scale systems.	13	K5	CO3
14.	a)	Apply the principles of two-level logic synthesis to design a simplified combinational circuit and demonstrate its optimization.	13	K3	CO4
		(OR)			
	b)	Use switch-level modeling techniques to simulate a CMOS inverter network and show how delay characteristics are obtained.	13	K3	CO4
15.	a)	Explain the role of allocation and scheduling in high-level synthesis and illustrate their interdependence with an example.	13	K2	CO5
		(OR)			
	b)	Describe high-level transformations and show how they support optimization in physical design automation.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Formulate a floor planning and routing methodology for a multi-core processor where modules vary in size and interconnect demand. Evaluate how your chosen approach balances area utilization, wire length, and congestion while meeting performance goals.	15	K5	CO3
		(OR)			
	b)	Design a VLSI CAD flow for a SoC used in autonomous vehicles, ensuring low power, reliable floor planning, efficient routing, and strict timing closure. Evaluate how partitioning, placement, routing, simulation, and synthesis choices enhance efficiency and scalability.	15	K5	CO3